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- 1 1. Instruction Set Architecture (ISA) selection logic
2 within a CPU for selecting an ISA decoding mode for a
3 program instruction from a plurality of ISA decoding
4 modes, the program instruction retrieved from an
5 address in an address space of the CPU, the selection
6 logic comprising:
7 a plurality of boundary address registers for storing
8 boundary addresses that partition the address
9 space into a plurality of address ranges
10 corresponding to the plurality of ISA decoding
11 modes; and
12 ISA mode selection logic, coupled to said plurality of
13 boundary address registers, for receiving the
14 address, and for comparing the address to said
15 boundary addresses to determine the ISA decoding
16 mode for the program instruction.
- 1 2. The selection logic as recited in claim 1, wherein the
2 CPU executes a multiple-ISA application program.
- 1 3. The selection logic as recited in claim 2, wherein said
2 multi-ISA application program comprises program
3 components having program instructions corresponding to
4 said plurality of ISA decoding modes.
- 1 4. The selection logic as recited in claim 3, wherein said
2 program instructions that correspond to a first ISA

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- 1 10. An Instruction Set Architecture (ISA) mode selection
 2 apparatus in a CPU, comprising:
 3 decoding logic, for decoding a program instruction
 4 retrieved from an address within an address space
 5 of the CPU;
 6 a boundary address register file, for storing boundary
 7 addresses that map one or more ISA modes of the
 8 CPU to corresponding address ranges within said
 9 address space; and
 10 an ISA mode controller, coupled to said boundary
 11 address register file, and to said decoding logic,
 12 for designating to said decoding logic an ISA mode
 13 to be used to decode said program instruction
 14 according to said address.
- 1 11. The ISA mode selection apparatus as recited in claim
 2 10, wherein said program instruction is within an
 3 application program that comprises components, each of
 4 said components having program instructions that
 5 correspond to only one of said one or more ISA modes.
- 1 12. The ISA mode selection apparatus as recited in claim
 2 11, wherein first program components corresponding to a
 3 first ISA mode are located within a first address
 4 range.

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- 1 13. The ISA mode selection apparatus as recited in claim
2 10, wherein said boundary address register file
3 comprises:
4 a plurality of boundary address registers, each storing
5 one of said boundary addresses.
- 1 14. The ISA mode selection apparatus as recited in claim
2 13, wherein said boundary addresses comprise lower
3 address boundaries for said corresponding address
4 ranges.
- 1 15. The ISA mode selection apparatus as recited in claim
2 14, wherein said ISA mode controller comprises address
3 evaluation logic for determining which one of said
4 plurality of boundary address registers corresponds to
5 said program instruction.
- 1 16. The ISA mode selection apparatus as recited in claim
2 15, wherein said ISA mode controller designates to said
3 decoding logic said ISA mode based upon determining
4 which one of said plurality of boundary address
5 registers corresponds to the program instruction.
- 1 17. The ISA mode selection apparatus as recited in claim
2 10, wherein said ISA mode controller provides said ISA
3 mode to said decoding logic to enable correct
4 processing of said program instruction.

1 18. A CPU for executing a multiple-ISA program, comprising:
2 ISA mode selection logic, configured to provide a first
3 ISA mode indicator that corresponds to a first
4 program instruction, said first program
5 instruction being fetched from a first address in
6 memory;
7 ISA mode boundary address registers, coupled to said
8 ISA mode selection logic, configured to store
9 boundary addresses that partition said memory into
10 address ranges, wherein a plurality of ISA modes
11 is mapped to said address ranges; and
12 an instruction decoder, coupled to said ISA mode
13 selection logic, configured to receive said first
14 ISA mode indicator, and configured to decode said
15 first instruction according to said first ISA
16 mode.

1 19. The CPU as recited in claim 18, wherein the multiple-
2 ISA program comprises components that are stored within
3 a corresponding address range.

A12
1 21. The CPU as recited in claim 20, wherein said boundary
2 addresses comprise lower address boundaries for said
3 address ranges.

1 22. The CPU as recited in claim 21, wherein said ISA mode
2 selection logic determines which one of said ISA mode
3 boundary address registers corresponds to first
4 address.

1 23. The CPU as recited in claim 22, wherein said ISA mode
2 selection logic provides said first ISA mode indicator
3 to said instruction decoder to enable correct
4 processing of said first program instruction.

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1 24. A computer program product for use with a computing
2 device, the computer program product comprising:
3 a computer usable medium, having computer readable
4 program code embodied in said medium, for causing
5 a CPU to be described, said CPU for executing a
6 multiple-ISA application program, said computer
7 readable program code comprising:
8 first program code, for providing boundary address
9 registers, configured to partition an address
10 space of said CPU into address ranges, said
11 address ranges corresponding to associated
12 ISA modes; and

A12

13 second program code, for providing ISA mode
14 selection logic, configured to receive an
15 address from which a program instruction was
16 retrieved, and configured to compare said
17 address against said address ranges to
18 determine an ISA mode for processing said
19 program instruction.

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1 25. The computer program product as recited in claim 24,
2 wherein said multiple-ISA application program comprises
3 program components corresponding to said associated ISA
4 modes.

1 26. The computer program product as recited in claim 25,
2 wherein each of said boundary address registers
3 contains an address boundary for a corresponding
4 address range.

1 27. The computer program product as recited in claim 26,
2 wherein said address boundary comprises a lower address
3 boundary for said corresponding address range.

1 28. The computer program product as recited in claim 27,
2 wherein said ISA mode selection logic determines a
3 particular boundary address register that corresponds
4 to said address.

A12

1 29. The computer program product as recited in claim 28,
2 wherein said ISA mode selection logic determines said
3 ISA mode that corresponds to said particular boundary
4 address register.

1 30. A method in a CPU for selecting an Instruction Set
2 Architecture (ISA) mode during execution of an
3 application program, the application program having
4 program instructions according to a plurality of ISA
5 modes, the method comprising:
6 a) partitioning an address space of the CPU into
7 address ranges, the address ranges being
8 designated by contents of a boundary register
9 file;
10 b) mapping each of the address ranges to each of a
11 plurality of ISA modes; and
12 c) selecting the ISA mode for processing of the program
13 instruction according to said mapping.

1 31. The method as recited in claim 30, wherein said
2 partitioning comprises:
3 i) specifying address boundaries within registers in
4 the boundary register file.

A12
1 32. The method as recited in claim 30, wherein said mapping
2 comprises:

3 i) storing individual components of the application
4 program within an associated address range that is
5 designated for processing of program instructions
6 corresponding to an associated ISA mode.

1 33. The method as recited in claim 32, wherein said mapping
2 further comprises:

3 ii) evaluating an address of a program instruction
4 fetched during execution of the application
5 program against the contents of the boundary
6 register file to determine a particular address
7 range within which the program instruction lies.

1 34. A computer data signal embodied in a transmission
2 medium, comprising:

3 first computer-readable program code, for providing
4 boundary address registers, said registers being
5 configured to partition an address space into
6 address ranges, said address ranges corresponding
7 to associated ISA modes.

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